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**[4857]-1073**

**S.E. (Computer Engineering) (First Semester)**

**EXAMINATION, 2015**

**DIGITAL ELECTRONICS AND LOGIC DESIGN**

**(2012 PATTERN)**

**Time : Two Hours**

**Maximum Marks : 50**

- N.B. :-** (i) Answer Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4,  
Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8.  
(ii) Figures to the right indicate full marks.  
(iii) Assume suitable data, if necessary.

1. (a) Implement each expression with NAND logic : [4]  
(i)  $ABC + DE$   
(ii)  $ABC + D' + E'$ .  
(b) Convert the decimal number 650 to hexadecimal by repeated division by 16. [2]  
(c) Draw three input standard TTL NAND gate circuit and explain its operation. [6]

*Or*

2. (a) Using K-map convert the following standard POS expression into a minimum POS expression, a standard SOP expression and minimum SOP expression : [6]

$$(A' + B' + C + D) (A + B' + C + D) (A + B + C + D') \\ (A + B + C' + D') (A' + B + C + D') (A + B + C' + D).$$

P.T.O.

(b) Prove the following rules of Boolean algebra : [2]

(i)  $A + A' B = A + B$

(ii)  $(A + B) (A + C) = A + BC.$

(c) Explain the advantages of open collector output. [4]

3. (a) Design a synchronous counter for

$$4 \rightarrow 6 \rightarrow 7 \rightarrow 3 \rightarrow 1 \rightarrow 4 \dots$$

Avoid lockout condition. Use JK flip-flop for design. [6]

(b) What are the full adder's inputs that will produce each of the following outputs ? [2]

(i)  $\Sigma = 0, C_{out} = 0$

(ii)  $\Sigma = 1, C_{out} = 0$

(iii)  $\Sigma = 1, C_{out} = 1$

(iv)  $\Sigma = 0, C_{out} = 1.$

(c) Explain the logic required to convert 6-bit binary number to gray code. Use that logic to convert the following binary numbers to gray code : [4]

(i) 101010

(ii) 111111

(iii) 000111

(iv) 111000.

*Or*

4. (a) Design a SEQUENCE DETECTOR using JK Flip-Flop to detect the following sequence. .... 1001 ..... Use state table diagram, state transition table and K-map as design tools. Remove all redundant states and draw the final circuit diagram. [6]

- (b) Determine the output for the following input states : [2]  
 $D_0 = 0, D_1 = 1, D_2 = 1, D_3 = 0, s_0 = 1, s_1 = 0.$   
Use 4 : 1 MUX.
- (c) Add the following BCD numbers : [4]
- (i) 1000 + 0110
  - (ii) 0111 + 0101
  - (iii) 0111 + 0010
  - (iv) 1000 + 0001.

5. (a) What is ASM chart ? Give its application and explain the MUX controller method with the suitable example. [6]
- (b) What is VHDL ? Write a VHDL code for 3 : 8 decoder using behavioral modeling style. [7]

*Or*

6. (a) Explain different modeling styles used in VHDL language with example. [6]
- (b) Draw an ASM chart for the 2-bit counter with the following specifications :
- (i) It will count UP if  $X = 1$
  - (ii) It will maintain the state if  $X = 0$
  - (iii) Produces output = 1.

If the counter bits are equal unconditionally, otherwise output = 0 unconditionally. X is an external input. [7]

7. (a) Show how PAL is programmed for the following 3 variable logic function : [6]
- (i)  $X = AB'C + A'BC' + A'B' + AC$
- (ii)  $Y = A'B'C + AB'C' + A + AB.$
- (b) What is FPGA ? Explain in detail the architecture of FPGA. [7]

*Or*

8. (a) What is the difference between PAL and PLA with suitable example ? [6]
- (b) Design a BCD to Excess-3 code converter and implement using suitable PLA. [7]